An 11 W Ku-band Heterostructure FET with WSi/Au T-shaped Gate

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ABSTRACT

We developed a Heterostructure FET (HFET) with a high output power and a high power-added efficiency (PAE) at Ku-band. 8 W and 11.2 W output powers were obtained with power-added efficiencies of 48% and 41% and linear gains of 9 dB and 8.6 dB at 12 GHz, respectively. This is the highest power and efficiency ever reported which is achieved by a single FET chip at this frequency.

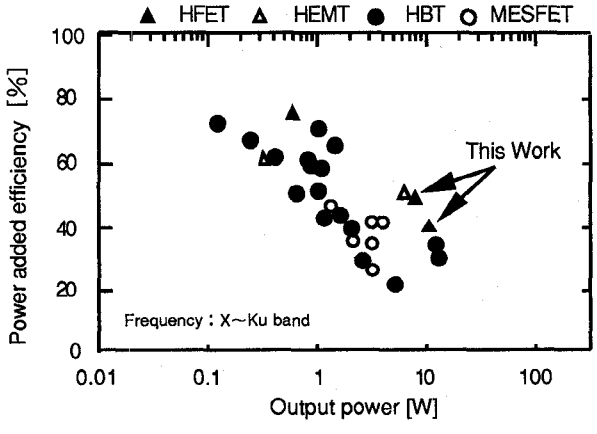

Fig.1 Power performance of a transistor at X-Ku band.

I. INTRODUCTION

Demands for high power amplifiers are increasing in microwave communication applications. Much work has been done to improve RF performances, especially output power and power-added efficiency of HFETs, HEMTs, and HBTs at X to Ku-band[1-3]. Both HEMTs and HBTs have high gain and high power density. However, there is not enough data concerning reliability, especially for several watts power class transistiors. From the viewpoint of reliability, refractory metal gates are suitable for high power applications because of their thermal stability[4]. We are developing a GaAs power FET with a sub-half micron WSi/Au T-shaped gate that has higher reliability than Al gate MESFETs[5].

In this paper, we describe an HFET with a sub-half micron WSi/Au T-shaped gate. As shown in Fig.1, it delivers the highest output power and power-added efficiency among single FETs at 12 GHz.

II. DEVICE DESCRIPTION

A schematic cross-section of a developed HFET

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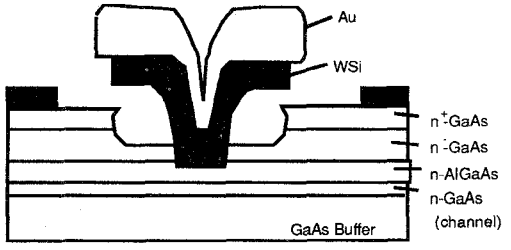

Fig.2 Schematic cross-section of an HFET with a buried gate.

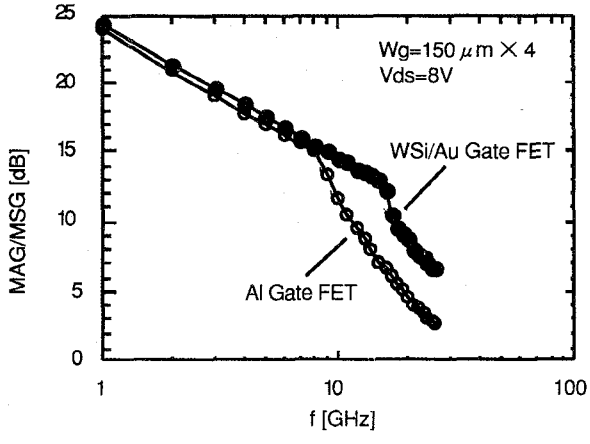

Fig.3 MAG/MSG as a function of frequency.

with a buried gate is shown in Fig.2. The HFET includes a high doped GaAs layer sandwiched between a superlattice buffer layer on the bottom and a low doped AlGaAs layer. We formed the WSi/Au T-shaped gate by using SiO_2 sidewalls[5]. The gate length is typically 0.4 μm. The WSi of the WSi/Au is employed as a schottky metal for high reliability and the Au is for reducing gate resistance. In order to reduce the influence of surface depletion, a buried gate structure was employed.

Figure 3 shows Maximum Available Gain and Maximum Stable Gain (MAG/MSG) of a WSi/Au gate FET and a conventional Al gate FET as a function of frequency. Because of the reduction of gate resistance, MAG of the WSi/Au gate FET is as high as 13.9 dB at 12 GHz, which is 4.3 dB higher than that of the Al gate

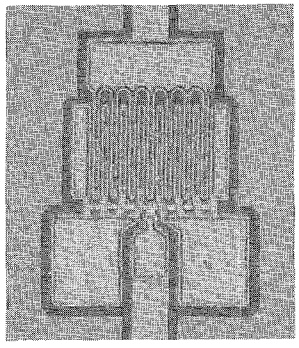

Fig.4 A 2.1mm gate periphery device.

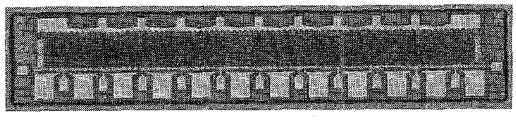

Fig.5 A 23.1mm gate periphery device.

FET.

The unit FET that was used for power application at Ku-band is the 2.1 mm gate periphery device shown in Fig.4. The unit gate width Wgu is 150 μm. To reduce the thermal resistance, the thickness of a GaAs substrate was thinned down to 30 μm and an Au plated heat sink (PHS) structure was adopted. The device that was used for power application is the 23.1 mm gate periphery (2.1 mm FET× 11) device shown in Fig.5. The chip size is 0.58× 2.75 mm^2.

In order to derive high output power, maximum drain current (Imax) should be large. Figure 6 shows the Imax of an HFET and a MESFET as a function of saturation current (Idss). Since the Imax of an HFET is larger than that of a MESFET, an HFET is expected to have a higher output power density. As shown in Fig.6, the Imax of an HFET saturates when the Idss is more than 200 mA/mm. So the most suitable value of the Idss is

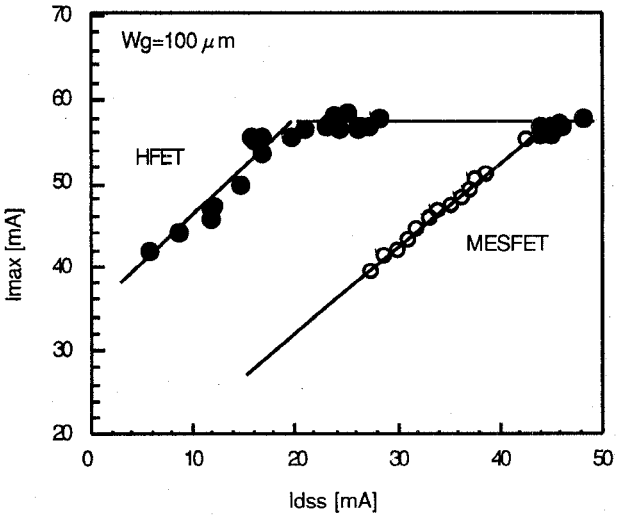

Fig.6 Imax versus Idss of an HFET and a MESFET.

200 mA/mm. We decided on Idss 200~300 mA/mm to avoid fluctuation.

III. CIRCUIT DESIGN

It is very difficult to measure the S-parameters of the 23.1 mm gate periphery FET precisely by the on-wafer probing technique, because the input and output impedance becomes too low. So we measured S-parameters of the 2.1 mm gate periphery FET , then calculated the S-parameters of the 23.1 mm gate periphery FET for matching circuit design. A Ku-band power module is shown in Fig.7. The module size is 21.0 × 12.9 mm^2. The input and output matching circuits consist of a 0.38 mm thick alumina microstrip circuit and a 0.1 mm thick high dielectric constant Barium Titanate ($BaTiO_3$, ε_r=38) microstrip circuit. For uniform operation of all unit FETs, it is necessary to make each wire length equal. Thus, the line width on the high dielectric substrate should be wider than the distance between gate pads. However, an undesirable propagation mode appears and reduces the output power when the

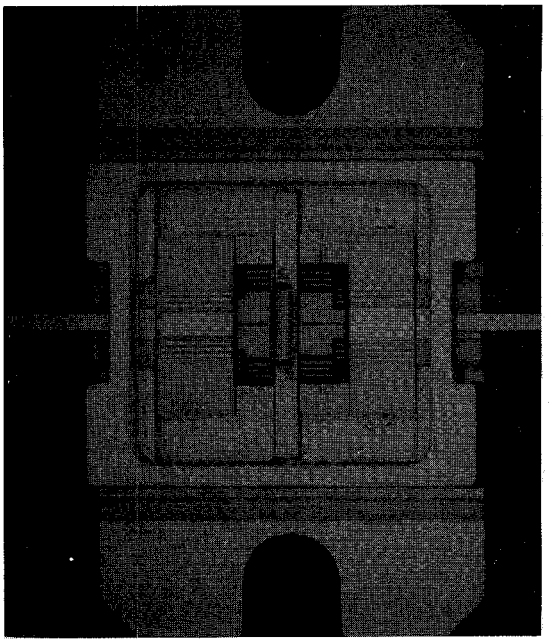

Fig.7 Ku-band power module.

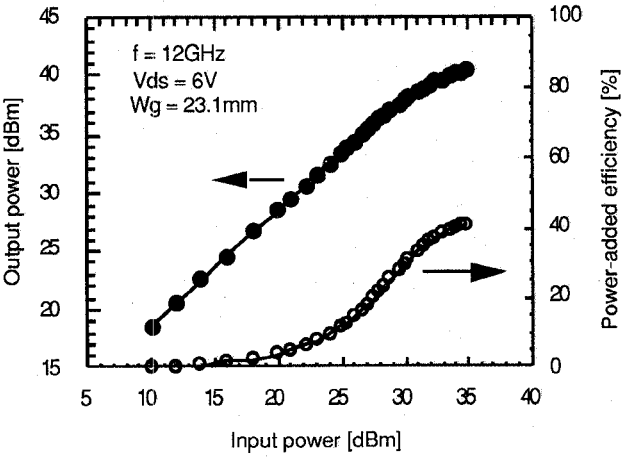

Fig.8 Measured power-added efficiency and output power as a function of input power.

width of the microstrip line becomes larger than halfof the wave length. Therefore, a slit was formed in the microstrip line of the high dielectric substrate. Gate and drain bias circuits are provided on both sides of the module using bias T network.

IV. PERFORMANCE

The gate-drain breakdown voltage (Vgdo) was typically 12∼14 V at a reverse current of 100 μA/mm. The Idss of an HFET was typically 250∼300 mA/mm. The transconductance was typically 200∼250 mS/mm.

The power characteristics of the 23.1 mm HFET were measured at 12 GHz. Figure 8 shows the output power and power-added efficiency for the 23.1 mm HFET. An 11.2 W output power was obtained with a PAE of 41% and a linear gain of 8.6 dB at 12 GHz. The power density is 480 mW/mm. An 8 W output power was obtained with a PAE of 48% and a linear gain of 9 dB at 12 GHz. This is the highest power and efficiency ever reported which is achieved by a single FET at this frequency.

Figure 9 shows the third-order intermodulation distortion (IMD_3) characteristics of the HFET. The frequency separation of the two tones is 5 MHz. The carrier-to-third-order intermodulation distortion ratio was as high as 29.0 dBc at 3 dB input backoff.

As shown in Fig.6, the Imax for an HFET is more than twice as much as the Idss, different from that of a MESFET. These results indicate that HFETs operate at a smaller Idss and a larger transconductance than MESFETs with the same output power. Thus, an HFET has an advantage over a MESFET for power applications.

V. CONCLUSION

We developed an HFET with a high power and a high efficiency at Ku-band. 8 W and 11.2 W output powers were obtained with power-added efficiencies of 48% and 41% and linear gains of 9 dB and 8.6 dB at 12 GHz, respectively. This is the highest power and efficiency ever reported which is achieved by a single FET chip at this frequency.

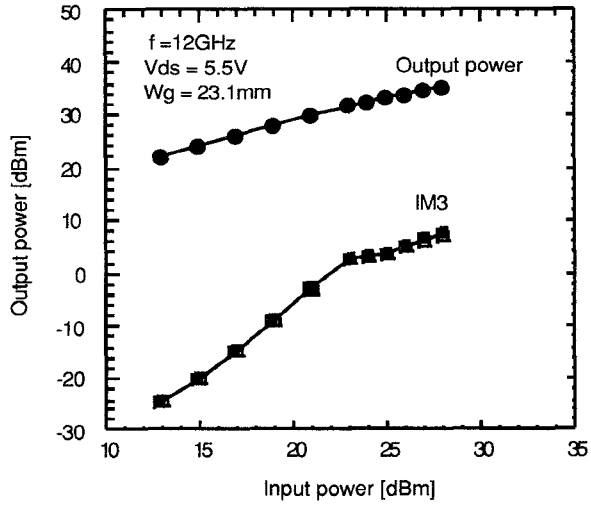

Fig.9 IM3 and output power as a function of input power.

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